processing mode, and the analog circuitry configured and arranged to capture and process data during a first data-communication interval while the digital signal processing circuitry is in the reduced activity mode; and

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means for effectively disabling the capture and processing of data by the analog circuitry during a second shorter data-communication interval while processing the data with the digital signal processing circuitry.

24. (*Amended*) In a communication arrangement having analog circuitry and digital signal processing circuitry, the analog circuitry coupled to receive streams of data presented thereto in the form of high-frequency signals for subsequent processing by the digital signal processing circuitry, a method for reducing noise passed from the digital signal processing circuitry to the data, comprising the steps of:

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using the analog circuitry to capture, process and to store the data during a first data-communication interval while the digital signal processing circuitry is in a reduced activity mode; and

disregarding additional data in the streams of data presented to the analog circuitry during a second shorter data-communication interval while processing the stored data with the digital signal processing circuitry.

Remarks

The Office Action mailed July 2, 2002, indicated that Claims 2-5 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention; Claims 1, 6-8, 11-15, 18-20 and 25-26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over *Cooper et al.* (U.S. Patent No. 5,294,928); Claims 2-5 and 23-24 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the '928 reference in view of *Narvinger et al.* (U.S. Patent No. 6,381,229); Claims 9-10 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the '928 reference in view of *Nordling* (U.S. Patent No. 6,138,190); Claims 16-17 and 21-22 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the '928 reference in view of *Berthoumieux* (E.P. Patent Document No.

447302A); Claims 27-28 stand rejected under 35 U.S.C. §103(a) as being unpatentable over the '928 reference in view of the '229 reference and the 447302A reference.

In addition, copies of references under the "OTHER DOCUMENTS" subheading of the IDS filed 11/16/99 were requested for consideration, the drawings were objected to for lack of reference numbers, claims 1-10 were objected to for informalities and claims 24 and 25 will be objected to should claims 23 and 18 be found allowable respectively. Claims 1-29, as amended, remain pending in the application and are presented for favorable reconsideration and allowance.

Applicant respectfully traverses each of the §112, second paragraph, and §103(a) rejections.

With respect to the IDS "OTHER DOCUMENTS" references, a supplemental IDS and copies of the available referenced IDS documents are included with this transmittal.

With respect to the drawing objections, Applicant proposes a drawing correction to Figure 5. More particularly within Channel 0, reference number 534 has been added to the top "Matched Filter" and reference number 544 has been added to the bottom "Matched Filter". A copy of the proposed drawing correction is attached noting the reference number insertions in red. Applicant respectfully submits the proposed drawing changes.

With respect to the objection to Claims 1-10, Applicant respectfully requests the objections be withdrawn. Claims 1 and 9-10 have been amended with this response.

With respect to the §112, second paragraph rejection of Claims 2-5, Applicant has amended Claim 2, and respectfully submits that the above-mentioned claims are not indefinite, and do particularly point out and distinctly claim the subject matter which Applicant regards as the invention in full satisfaction of § 112, second paragraph. Therefore, Applicant requests that the §112, second paragraph, rejection of Claims 2-5 be withdrawn.

With respect to the § 103(a) rejection of Claims 1, 6-8, 11-15, 18-20 and 25-26, it is respectfully submitted that the rejection is improper because it fails to establish a *prima facie* case of obviousness based on the modification of the '928 reference. To establish a

facie case of obviousness based on the modification of the '928 reference. To establish a *prima facie* case of obviousness based on a modification of a primary reference, three basic criteria must be met, as is set forth in M.P.E.P. §2143:

1) The prior art references must teach or suggest all of the claim limitations; and
2) There must be some suggestion or motivation, either in the reference itself or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings; and
3) There must be a reasonable expectation of success.

The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure. *See In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d 1438 (Fed. Cir. 1991). Further, the prior art must suggest the desirability of the combination of the references. *In re Mills*, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1990).

With particular respect to the § 103(a) rejection of independent Claim 1 and the claims depending therefrom, the cited reference does not addresses the same problem as the claimed invention, or show all aspects claimed and therefore, the reference cannot be used to maintain the rejection under § 103(a). Specifically, Applicant fails to see among the cited reference portions, *inter alia*, a teaching or suggestion of features completely corresponding to the claimed limitations of in a mode other than the reduced-activity mode and during a second shorter time interval, clocking the digital signal processing circuitry to permit digital signal processing of the captured information data. The Office Action concedes that Cooper does not expressly teach the claim as a whole, because the cited reference is missing a claimed limitation. The Office Action does not even allege that the missing feature is "known." Instead, the Office Action asserts that one of ordinary skill in the art would recognize that different periods of time would be necessary to perform the analog operations and the digital operations depending on the application. However, this generalization of the present invention fails to view the invention "as a whole," as required by § 103(a), and is based impermissible hindsight after having benefit of Applicant's disclosure. Suggesting that the motivation to modify a cited reference

attempt to justify virtually any type of modification and does not provide motivation for making the specific modification asserted. The Examiner's argument is merely an attempt to simply ignore the missing claimed limitation.

To the extent that the Examiner is attempting to make an inherency argument, such an argument cannot be sustained by speculation. In order to establish inherency, the extrinsic evidence "must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *Continental Can Co. v. Monsanto Co.*, 948 F.2d 1264, 1268, 20 USPQ2d 1746, 1749 (Fed. Cir. 1991) (emphasis added). "Inherency, however, may not be established by probabilities or possibilities. The mere fact that a certain thing may result from a given set of circumstances is not sufficient" (emphasis added). *Id* at 1269, 20 USPQ2d at 1749 (quoting *In re Oelrich*, 666 F.2d 578, 581, 212 USPQ 323, 326 (C.C.P.A. 1981). In this instance, although the Examiner does not expressly argue that the claimed invention is inherent, if this argument were being impliedly asserted, it would be insufficient as a matter of law because the claimed invention, including the digital operations being a shorter time interval and occurring during a mode other than during the analog operations, is not inherently present in the asserted reference.

More particularly, that different time periods may be necessary to perform analog and digital operations does not teach or suggest that the respective operations be done in separate and distinct, mutually exclusive modes, or teach or suggest that the digital operations mode be during a shorter time interval. In fact, the '928 reference teaches away from the claimed invention. Not only does the '928 reference teach the digital circuitry sleeping after sampling of the analog input signal (col. 3, lines 53-56), but the '928 reference requires that "the sampling phase must be performed with both the microcontroller and the ADC in an active state (non-sleep)" (col. 6, lines 37-41). Therefore, the '928 reference does not teach or suggest the claimed mode aspects, and the Office Action fails to establish a *prima facie* case of obviousness with respect to the claimed invention. Accordingly, Applicant requests that the § 103(a) rejection of independent Claim 1, and all claims depending therefrom, be removed.

With particular respect to Claim 7, Applicant fails to see among the cited reference portions, *inter alia*, a teaching or suggestion of features completely corresponding to the claimed limitations of the first interval being substantially greater than the second interval. The Office Action does not allege that the first (analog) interval being substantially greater than the second (digital) interval, even if analog and digital operations are "different periods of time," and thus fails to establish a *prima facie* case of obviousness with respect to the claimed invention. Accordingly, Applicant requests that the § 103(a) rejection of independent Claim 7 be removed.

With particular respect to independent Claims 11, 18, 23-24 and 25, and the claims depending respectively therefrom, Applicant fails to see among the cited reference portions, *inter alia*, a teaching or suggestion of features completely corresponding to the claimed limitations of means for effectively disabling the processing of data by the analog circuitry during a second shorter data-communications interval while processing the data with the digital signal processing circuitry. The '928 reference appears to teach a situation in which the system effectively disables the processing of data by digital circuitry (*e.g.*, a microcontroller) while processing data with the ADC. Therefore, the Office Action fails to establish a *prima facie* case of obviousness with respect to the claimed invention and Applicant requests that the § 103(a) rejection of independent Claims 11, 18 and 25, and all claims depending respectively therefrom, be removed.

With particular respect to Claim 26, Applicant traverses the Examiner's assertion that the at least 90% and no more than 10% processing times for analog and digital processing respectively is a design consideration, and requests that a supporting citation of some reference work for said feature be provided if the rejection is to be maintained. *See In re Ahlert*, 424 F.2d 1088, 1091, 165 USPQ 418, 420-421 (CCPA 1970) ("[A]ssertions of technical facts in areas of esoteric technology must always be supported by citation of some reference work" and allegations concerning specific 'knowledge' of the prior art, which might be peculiar to a particular art should also be supported"). *See also*, MPEP §2144.03. Alternatively, Applicant requests that the § 103(a) rejection of Claim 26 be removed.

With particular respect to Claims 2-5, 9-10, 16-17 and 21-22, which depend from independent Claim 1, were also rejected under 35 U.S.C. §103(a) as being unpatentable over the '928 reference. While Applicant does not acquiesce with respect to any particular rejections applied to these dependent claims, it is believed that these rejections are now moot in view of the remarks made in connection with independent Claim 1. These dependent claims include all of the limitations of the base claim and any intervening claims, and recite additional features which further distinguish these claims from the cited references. "If an independent claim is nonobvious under 35 U.S.C. §103, then any claim depending therefrom is nonobvious." M.P.E.P. §2143.03 *citing In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988). Therefore, dependent Claims 2-5 and 9-10 are also allowable.

With further particular respect to Claims 2-5, and 27-28, the Office Action concedes that the '928 reference does not teach shutting off the analog circuitry occurring during a known guard time (¶ 10, p.5). However, the Office Action suggests that the '229 reference teaches a guard interval during which time dummy information is transmitted, asserts that such dummy information "does not have to be detected and processed by the receiver" and concludes that "[i]t would have been obvious to one of ordinary skill in the art to combine the teachings of Cooper and Narvinger by disabling the analog portion of a receiver during a guard period where no data is transmitted." First, the '229 reference does not appear to associate modify operation of the receiver during the guard period – this is merely an unsupported assertion based on impermissible hindsight after having the disclosure of the present invention. In addition, the '229 reference teaches away from the Examiners suggestion of "disabling the analog portion of a receiver during a guard period" since the '229 reference teaches advantageously using the information transmitted during the guard period (col. 13, lines 1-21). Therefore, the asserted references fail to establish a *prima facie* case of obviousness with respect to the claimed invention.

Furthermore, the misguided effort to find complete correspondence between the asserted prior art and the claimed invention lacks motivation and attempts only to satisfy the first component of the *prima-facie* obviousness test. The Examiner failed to specifically identify "clear and particular" reasons that indicate why one of ordinary skill

in the art would have been motivated to select the missing claim limitations and modify the underlying reference with them. *See, e.g., In re Dembiczak*, 175 F.3d 994, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999). Further, the Examiner failed to provide some actual evidence of a suggestion, teaching or motivation to combine references found in the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved that would suggest the combination, or show some objective teaching leading to the combination. *See In re Fine*, 837 F.2d 1071, 1075, 5 USPQ2d 1596, 1600 (Fed. Cir. 1988). Therefore, in also failing to satisfy the motivation requirement, the Office Action further fails to establish a *prima facie* case of obviousness with respect to the claimed invention, and Applicant requests that the § 103(a) rejection of Claims 2-5 be removed.

With further particular respect to Claims 16-17 and 21-22, the Office Action concedes that "Cooper fails to disclose that the analog circuitry includes a means for receiving low-energy, high-frequency data, and that both the analog and digital circuitry can receive and transmit data" and asserts that the 447302A reference teaches the missing features. However, the asserted combination of references lacks motivation, and thus fails to establish a *prima facie* case of obviousness. The conclusory statement that it would have been obvious to combine the asserted references "so bi-directional communication between two radio communication devices may be established" is again impermissible hindsight based on the Applicant's disclosure for modifying a semiconductor microcontroller with the capability to perform analog to digital conversions (Abstract) of the '928 reference with a time-multiplexed radio communications device of the 447302A reference. The Examiner failed to provide actual evidence of a suggestion, teaching or motivation to combine references found in the references themselves, the knowledge of one of ordinary skill in the art, or from the nature of the problem to be solved that would suggest the combination. *See In re Fine*. A combination of references based so clearly on impermissible hindsight fails to satisfy the motivation requirement, thus failing to establish a *prima facie* case of obviousness with respect to the claimed invention. Accordingly, Applicant requests that the § 103(a) rejection of Claims 16-17 and 21-22 be removed.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Reconsideration and withdrawal of the rejections, along with a favorable response, are earnestly requested.

No fees are believed required with this response. No fees are believed required with the supplemental IDS as we are providing the references per the Examiner's request.

Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is encouraged to contact the undersigned at (651) 686-6633.

Respectfully submitted,

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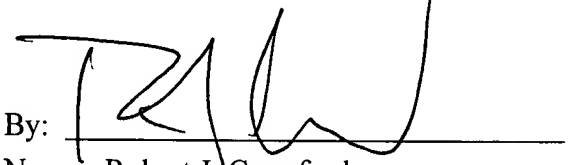
By: 

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Claim Changes for S/N 09/310,598

1. (*Amended*) In a communication arrangement having analog circuitry and having digital signal processing circuitry clocked sufficiently fast to generate noise, the analog circuitry susceptible to processing corrupted data due to the noise coupled thereto, a method for reducing noise passed from the digital signal processing circuitry, comprising the steps of:

using the analog circuitry to capture information data from an incoming stream for [at] a first time interval while the digital signal processing circuitry is in a reduced-activity mode; and

in a mode other than the reduced-activity mode and during a second shorter time interval, clocking the digital signal processing circuitry to permit digital signal processing of the captured information data.

2. (*Amended*) A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, wherein the mode other than the reduced-activity mode [step of effectively disabling the processing of data by the analog circuitry while processing the data with the digital signal processing circuitry] occurs during a known guard time for the data being communicated to the communication arrangement.

9. (*Amended*) A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, further including the steps of: providing a memory circuit coupled for access by at least a portion of the [analogy] analog circuitry and by at least a portion of the digital signal processing circuitry; using said at least a portion of the analog circuitry to read data out of the memory circuit and using said at least a portion of the digital signal processing circuitry to write data into the memory circuit.

10. (*Amended*) A method for reducing noise passed from the digital signal processing circuitry, according to claim 1, further including the steps of: providing a

memory circuit coupled for access by at least a portion of the [analogy] analog circuitry and by at least a portion of the digital signal processing circuitry; using said at least a portion of the analog circuitry to write data into the memory circuit and using said at least a portion of the digital signal processing circuitry to read data out of the memory circuit.

18. (*Amended*) A communication arrangement susceptible to processing corrupted data due to noise coupled thereto via high-speed data processing, comprising:

a chip including both digital signal processing circuitry and analog circuitry, the digital signal processing circuitry having a reduced activity mode and a high-speed data processing mode, and the analog circuitry configured and arranged to capture and process data during a first data-communication interval while the digital signal processing circuitry is in the reduced activity mode; and

means for effectively disabling the capture and processing of data by the analog circuitry during a second shorter data-communication interval while processing the data with the digital signal processing circuitry.

24. (*Amended*) In a communication arrangement having analog circuitry and digital signal processing circuitry, the analog circuitry coupled to receive streams of data presented thereto in the form of high-frequency signals for subsequent processing by the digital signal processing circuitry, a method for reducing noise passed from the digital signal processing circuitry to the data, comprising the steps of:

using the analog circuitry to capture, process and to store the data during a first data-communication interval while the digital signal processing circuitry is in a reduced activity mode; and

disregarding additional data in the streams of data presented to the analog circuitry during a second shorter data-communication interval while processing the stored data with the digital signal processing circuitry.